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L10	370	(matrix or matrices or vector\$1) and 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/05 13:08
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United States Patent Application: 0030208661

... Kind Code, A1. Magoshi, Hidetaka, November 6, 2003. Methods and apparatus for controlling a cache memory Abstract. ... Inventors: Magoshi, Hidetaka; (Palo Alto, CA). ... appft1.uspto.gov/netaogi/nph-Parser?Sect1=PTO2& Sect2=HITOFF&p=1&u=%2Fnetahtmi%2FPTO%2Fsearch-... - 61k - Coched - Similar pages

United States Patent Application: 0030177343

... (17 of 25). United States Patent Application, 20030177343. Kind Code, A1. Magoshi, Hidetaka, September 18, 2003. ... Inventors: Magoshi, Hidetaka; (Palo Alto, CA). ... applif1.uspto.gov/netacgi/nph-Parser?Seot1=PTO2& Sect2=HITOFF&p=1&u=%2Fnetahtmi%2FPTO%2Fsearch- ... - 62k - Cached - Similar pages
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US Pregrants in Class 711/217 - Generating a particular pattern ...

... 20040003178, 2004-1-1, Methods and apparatus for controlling a cache memory, Magoshi, Hidetaka. 2004 Paterra, Inc. Original IPC schedule from WIPO. cxp.paterra.com/uspregrantsc711s217000.html - 12k - Supplemental Result - Cached - Similar pages

EP1211615

... 20011008 Requested Patent: [_] EP1211615 Applicant(s): SONY COMP ENTERTAINMENT INC (JP) Inventor(s): SASAKI NOBUO (JP); **MAGOSHI HIDETAKA** (JP) Publication date ... swpat.ffii.org/pikta/txt/ep/1211/615/ - 46k - Jan 3, 2005 - Cached - Similar pages

Electronics Times: Sony plans loss-leader chip strategy (Product ...

... Demonstrating the Emotion Engine (EE) and Graphics Synthesiser (GS) chips at the Embedded Processor Forum, **Hidetaka Magoshi**, vice- president of LSI development ... www.findarticles.com/cf_dis/ m0V/VI/1999_May_10/54620121/p1/article.jhtml - 11k - Supplemental Result - <u>Ceched - Similar pages</u>

Electronic News: Simplex rolls SI tools: Library characterization ...

... at gate-level speed, played an important role in first-pass timing closure for our Graphics Synthesizer I-32 chip," said **Hidetaka Magoshi**, vice president of ... www.findarticles.com/cf_dis/ m0EKF/9_46/83353855/p1/article.jhtml - 13x - Supplemental Result - <u>Cached - Similar pages</u> [More results from www.findarticles.com]

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... challenge in trying to build a chip of this size, almost 300 million transistors integrated onto a single chip," said **Hidetaka Magoshi**, vice president ... www.edac.org/downloads/pressreleases/presst_PR15.htm - 53k - <u>Cached</u> - <u>Similar pages</u>

Hot Chips 14 - A Symposium on High Performance Chips at Stanford ...

... Microsystems. BREAK | 3:00 pm - 3:30 pm. SESSION 4 | Technology | 3:30 pm - 5:00 pm | Chair: Hidetaka Magoshi. • Integrated Cryptographic ... www.hotchips.org/hc14/finalprogram.html - 28k - Cached - Similar pages

TFCC

... 3b. Title: Sony Playstation 2 , Motivation, Requirements and Architecture Definition. Speaker: **Hidetaka Magoshi**, Sony Computer Entertainment. 3c. ... www.unf.edu/cceo/ieee/prev_vaii_1999.html - 25k - <u>Cached - Similar pages</u>

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1 A novel VLSI BiCMOS/bipolar concurrent multiplier-accumulator for DSP applications

Poornaiah, D.V.; Ananda Mohan, P.; Ahmad, M.O.; Bipolar/BiCOMS Circuits and Technology Meeting, 1993., Proceedings of the 1993, 4-5 Oct. 1993 Pages:171 - 174

[Abstract] [PDF Full-Text (480 KB)] IEEE CNF

2 Architectural optimizations for a floating point multiply-accumulate unit in a graphics pipeline

Acken, K.P.; Irwin, M.J.; Owens, R.M.; Garga, A.K.; Application Specific Systems, Architectures and Processors, 1996. ASAP 96. Proceedings of International Conference on , 19-21 Aug. 1996 Pages:65 - 71

[Abstract] [PDF Full-Text (300 KB)] IEEE CNF

3 Serial/Parallel architectures for area-efficient vector multiplication Smith, S.; Denyer, P.;

Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '87., Volume: 12, Apr 1987 Pages:539 - 542

[Abstract] [PDF Full-Text (152 KB)] IEEE CNF

4 Kerneltron: support vector "machine" in silicon

Genov, R.; Cauwenberghs, G.;

Neural Networks, IEEE Transactions on , Volume: 14 , Issue: 5 , Sept. 2003 Pages:1426 - 1434

[Abstract] [PDF Full-Text (1179 KB)] IEEE JNL

5 Dynamic range analysis for the implementation of fast transform

Xia Wan; Yiliang Wang; Chen, W.H.;

Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 5

, Issue: 2 , April 1995 Pages:178 - 180

[Abstract] [PDF Full-Text (216 KB)]

6 Array architecture for solving large-scale linear system of equations

by block Gauss-Seidel algorithm and local reordering approach

Chen, B.; Onoda, M.;

Communications, Computers and Signal Processing, 1989. Conference Proceeding., IEEE Pacific Rim Conference on , 1-2 June 1989 Pages: 56 - 59

[Abstract] [PDF Full-Text (292 KB)] IEEE CNF

7 Real-time linear-predictive coding of speech on the SPS-41 triple-microprocessor machine

Knudsen, M.;

Acoustics, Speech, and Signal Processing [see also IEEE Transactions on Signal Processing], IEEE Transactions on , Volume: 23 , Issue: 1 , Feb 1975 Pages:140 - 145

[Abstract] [PDF Full-Text (800 KB)] IEEE JNL

8 An algorithm-based error detection scheme for the multigrid method

Mishra, A.; Banerjee, P.;

Computers, IEEE Transactions on , Volume: 52 , Issue: 9 , Sept. 2003

Pages:1089 - 1099

[Abstract] [PDF Full-Text (859 KB)] IEEE JNL

9 Charge-mode parallel architecture for vector-matrix multiplication

Genov, R.; Cauwenberghs, G.;

Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on], Volume: 48, Issue: 10, Oct. 2001 Pages: 930 - 936

[Abstract] [PDF Full-Text (205 KB)] IEEE JNL

10 Fast parallel recursive aggregation methods for simulation of dynamical systems

Tsai, W.K.; Garng Huang; Wei Lu;

Automatic Control, IEEE Transactions on , Volume: 39 , Issue: 3 , March 1994

Pages:534 - 540

[Abstract] [PDF Full-Text (620 KB)] IEEE JNL

11 The CCD neural processor: a neural network Integrated circuit with 65536 programmable analog synapses

Agranat, A.J.; Neugebauer, C.F.; Nelson, R.D.; Yariv, A.;

Circuits and Systems, IEEE Transactions on , Volume: 37 , Issue: 8 , Aug. 1990

Pages:1073 - 1075

[Abstract] [PDF Full-Text (200 KB)] IEEE JNL

12 VLSI implementation of a 16×16 discrete cosine transform

Sun, M.-T.; Chen, T.-C.; Gottlieb, A.M.;

Circuits and Systems, IEEE Transactions on , Volume: 36 , Issue: 4 , April 1989

Pages:610 - 617

[Abstract] [PDF Full-Text (740 KB)] IEEE JNL

13 Design and Implementation of a GaAs systolic floating-point processing element

Beaumont-Smith, A.; Marwood, W.; Lim, C.C.; Eshraghian, K.; Computers and Digital Techniques, IEE Proceedings- , Volume: 143 , Issue: 5 , Sept. 1996

Pages: 325 - 330

[Abstract] [PDF Full-Text (628 KB)] IEE JNL

14 Design of a systolic array system for linear state equations

Jou, S.-J.; Jen, C.-W.;

Circuits, Devices and Systems, IEE Proceedings G [see also IEE Proceedings-Circuits, Devices, and Systems] , Volume: 135 , Issue: 5 , Oct.

Pages:211 - 218

[Abstract] [PDF Full-Text (508 KB)] IEE JNL

15 A reconfigurable low-power high-performance matrix multiplier design

Lin, R.;

Quality Electronic Design, 2000. ISQED 2000. Proceedings. IEEE 2000 First International Symposium on , 20-22 March 2000 Pages:321 - 328

[Abstract] [PDF Full-Text (108 KB)] IEEE CNF

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